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High Speed and Area Efficient Parallel Fir Digital Filter Structures for DSP Application Based on Fast Fir Algorithm

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Abstract

Finite impulse response (FIR) digital filters are one of the most widely used fundamental devices performed in DSP systems, ranging from wireless communications to video and image processing. This paper proposes new parallel FIR filter structures, which are beneficial to symmetric coefficients in terms of the hardware cost, under the condition that the number of taps is a multiple of 2 or 3. The 5 parallel FIR structures gives low area and high speed compare to existing 4 parallel architecture , exploit the inherent nature of symmetric coefficients reducing half the number of multipliers in sub filter section at the expense of additional adders in preprocessing and post processing blocks. Exchanging multipliers with adders is advantageous because adders weigh less than multipliers in terms of silicon area. Due to reduction of multipliers, will get low area and high speed fir filter.

Keywords: DSP, Fir Filter, FFA.

Introduction

ALONG the explosive growth of multimedia application, the demand for high-performance and low-power digital signal processing (DSP) is getting higher and higher. The FIR digital filter is one of the most widely used fundamental devices performed in DSP systems, ranging from wireless communications to video and image processing. Some applications need the FIR filter to operate at high frequencies such as video processing, whereas some other applications request high throughput with a low-power circuit such as multiple-input– multiple-output systems used in cellular wireless communication. Furthermore, when narrow transition band characteristics are required, the much higher order in the FIR filter is unavoidable. In this brief, parallel processing in the digital FIR filter will be discussed. Due to its linear increase in the hardware implementation cost brought by the increase in the block size L, the parallel processing technique loses its advantage to be employed in practice. There have been a few papers proposing ways to reduce the complexity of the parallel FIR filter in the past. In, poly phase decomposition is mainly manipulated, where the small-sized parallel FIR filter structures are derived first and then the larger block-sized ones can be constructed by cascading or by iterating small-sized parallel FIR filtering blocks. Fast FIR algorithms (FFAs) introduced in [1]–[3] show that they can implement an L-parallel filter using approximately (2L − 1) sub filter blocks, each of which is of length N/L. It reduces the required number of multipliers to (2N − N/L) from L × N . In the fast linear convolution is utilized to develop the small-sized filtering structures, and then a long convolution is decomposed into several short convolutions, i.e., larger block-sized filtering structures can be constructed through iterations of the small-sized filtering structures. However, in both categories of methods, when it comes to symmetric convolutions, the symmetry of coefficients has not been taken into consideration yet, which can lead to a significant saving in hardware cost. Previously, we have investigated the design for symmetric convolutions based on even length . In this brief, we will discuss symmetric convolutions based on odd length and provide new parallel FIR digital filter architectures consisting of advantageous poly phase decomposition, which can further reduce amounts of multipliers required in the sub filter section by exploiting the inherent nature of the symmetric coefficients, compared with the existing FFA fast parallel FIR filter structures. This brief is organized as follows. A brief introduction of FFAs. In Section III, the proposed parallel FIR filter architectures are presented.

FFA

Consider an N -tap FIR filter that can be expressed in the general form as

$$y(n) = \sum_{i=0}^{N-1} h(i)x(n-i), \qquad n = 0, 1, 2, \ldots, \infty$$

where x(n) is an infinite length input sequence and h (i) represents the length-N FIR filter coefficients. Then, the traditional L- parallel FIR filter can be derived using poly phase decomposition as

$$\sum_{p=0}^{L-1} Y_p(z^L)z^{-p} = \sum_{q=0}^{L-1} X_q(z^L)z^{-q} \sum_{r=0}^{L-1} H_r(z^L)z^{-r}$$

Two-parallel FIR filter implementation using the FFA

1). 2 × 2FFA (L =2)

According to (2), a two-parallel FIR filter can be expressed as

$$Y_0 = H_0X_0 + z^{-2}H_1X_1$$
$$Y_1 = H_0X_1 + z^{-2}H_1X_0.$$

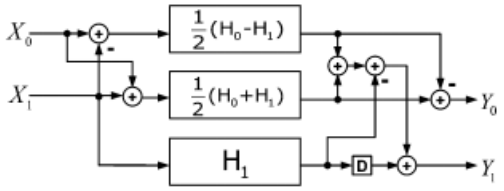


Fig.1 Two-parallel FIR filter implementation using the FFA

However, (3) can be written as

$$Y_0 = H_0X_0 + z^{-2}H_1X_1,$$
$$Y_1 = (H_0 + H_1)(X_0 + X_1) - H_0H_0 - H_1H_1.$$

The two-parallel (L =2) FIR filter implementation using the

FFA obtained from shown in Fig….

Three-parallel FIR filter implementation using the FFA

2). 3 × 3FFA (L =3)

For a set of symmetric coefficients in odd length N , when (N mo d 3) equals 1, such as N =25, the proposed structure 3B in i.e., presented as (8), can earn one more sub filter block with symmetric coefficients over the existing FFA

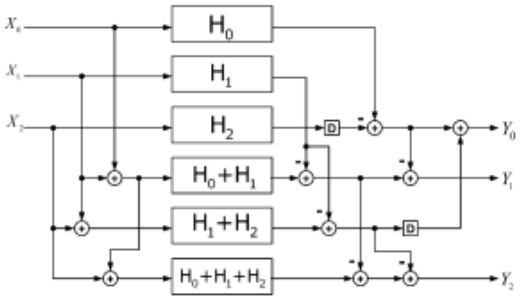


Fig .2. 3 × 3FFA (L =3)

By the similar approach, a three-parallel FIR filter using the FFA can be expressed a

$$Y_0 = H_0X_0 - z^{-3}H_2X_2 + z^{-3} \times [(H_1 + H_2)(X_1 + X_2) - H_1X_1]$$
$$Y_1 = [(H_0 + H_1)(X_0 + X_1) - H_1X_1] - (H_0X_0 - z^{-3}H_2X_2)$$
$$Y_2 = [(H_0 + H_1 + H_2)(X_0 + X_1 + X_2)] - [(H_0 + H_1)(X_0 + X_1) - H_1X_1] - [(H_1 + H_2)(X_1 + X_2) - H_1X_1].$$

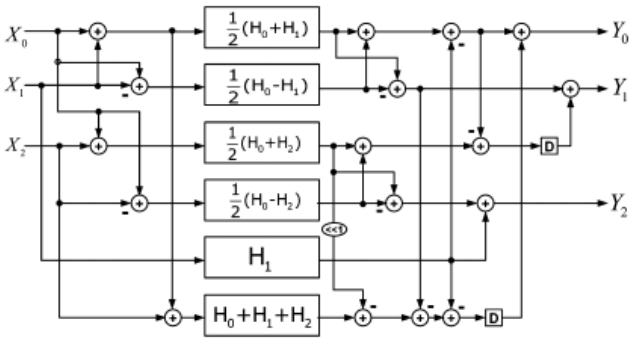


Fig.3 Proposed three-parallel FIR filter implementation.

The existing two-parallel FFA structure naturally has benefits to symmetric convolutions in odd length. When it comes to a set of odd-length symmetric coefficients, two out of three sub filters contain symmetric coefficients, i.e., H0 and H 1 ,shown in Fig. 1. However, the existing three-parallel FFA structure is not as advantageous. In this section, new three-parallel FIR filter structures are proposed, which enables more multipliers sharing in the sub filter section and, therefore, can save more hardware cost over the existing FFA.

Proposed Structure 3A, ((Nmod 3) = 0): From (5), it can also be presented as (7). For a set of symmetric coefficients in odd length N , when (N mo d 3) equals zero, (7) can earn two more sub filter blocks containing symmetric coefficients than (5).

The implementation of the proposed three-parallel FIR filter Each output of multipliers responds to two taps, except the middle one. Note that the transposed direct-form FIR filter is employed. Compared with the existing FFA three-parallel FIR filter structure, the proposed structure leads to two more sub filter blocks, which contains symmetric coefficients. A comparison figure is shown in Fig. 3, where the shadow blocks stand for the sub filter blocks, which contain symmetric coefficients. Therefore, for an N -tap three-parallel FIR filter, the proposed structure can save N/ 3 multipliers from the existing FFA structure. However, it comes with the price of the increase in amount of adders, i.e., five additional adders, in preprocessing and post processing blocks.

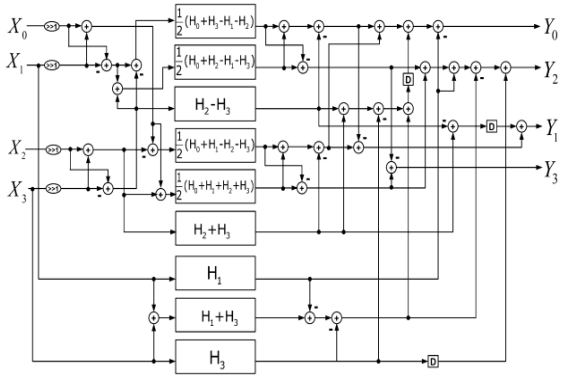


Fig.4 Four parallel FIR filter implementation

The proposed cascading process for the larger block-sized proposed parallel FIR filter is similar to that introduced in [1], but instead of applying the existing small-sized FFAs to every stage, we interleave multiple various small-sized structures in each stage to fully exploit the symmetry of coefficients. For two-parallel-based cascading, with a set of odd-length symmetric coefficients, it is possible to have even-length symmetric coefficients in a sub filter block after applying two-parallel FFA structure. For example, for a set of 23-tap symmetric coefficients, after applying two-parallel FFA, the sub filter block H0 is with 12 symmetric coefficients, to which the existing FFA is not beneficial. Therefore, in this case, the two-parallel structure that is advantageous to even-length symmetric coefficients is employed. The resulted four-parallel filter realization, which leads to four sub filter blocks containing

Proposed Cascading FFA

The proposed cascading process for the larger block-sized proposed parallel FIR filter is similar to that introduced in [1]. However, a small modification is adopted here for lower hardware consumption. As we can see, the proposed parallel FIR structure enables the reuse of multi-pliers in parts of the sub filter blocks but it also brings more adder cost in preprocessing and post processing blocks. When cascading the pro-posed FFA parallel FIR structures for larger parallel block factor the increase of adders can become larger. Therefore, other than applying the proposed FFA FIR filter structure to all the decomposed sub filter blocks, the existing FFA structures which have more compact operations in preprocessing and post processing blocks are employed for those sub filter blocks that contain no symmetric coefficients, whereas the proposed FIR filter structures are still applied to the rest of sub filter blocks with symmetric coefficients. An illustration of the proposed cascading process for a four-parallel FIR filter as an example is shown in Fig., and the realization is shown in Fig. 4. From Fig. , it is clear to see that the proposed four-parallel FIR structure earns three more sub filter blocks containing symmetric coefficients than the existing FFA one, which means multipliers can be saved for an tap FIR filter, at the price of 11 additional adders in preprocessing and post processing blocks. By this cascading approach, parallel FIR filter structures with larger block factor can be realized. The pro-posed six-parallel FIR filter will result in 6 more symmetric sub filter blocks, equivalently multipliers saved for an -tap FIR filter, than the existing FFA, at the expense of an additional 32 adders. Also, the proposed eight-parallel FIR filter will lead to seven more symmetric sub filter blocks, equivalently multipliers saved for an -tap filter, than the existing FFA, with the overhead of additional 54 adders.

$$
\begin{aligned}
Y_0 &= H_0X_0 - z^{-3}H_2X_2 + z^{-3} \\
&\quad \times [(H_1+H_2)(X_1+X_2) - H_1X_1] \\
Y_1 &= [(H_0+H_1)(X_0+X_1) - H_1X_1] \\
&\quad - (H_0X_0 - z^{-3}H_2X_2) \\
Y_2 &= [(H_0+H_1+H_2)(X_0+X_1+X_2)] \\
&\quad - [(H_0+H_1)(X_0+X_1) - H_1X_1] \\
&\quad - [(H_1+H_2)(X_1+X_2) - H_1X_1].
\end{aligned}
$$

$$\boldsymbol{Y_4 = \frac{1}{2}[(H_3+H_4)(X_3+X_4) - (H_3-H_4)(X_3 - X_4)] + (H_1+H_2)X_2}$$

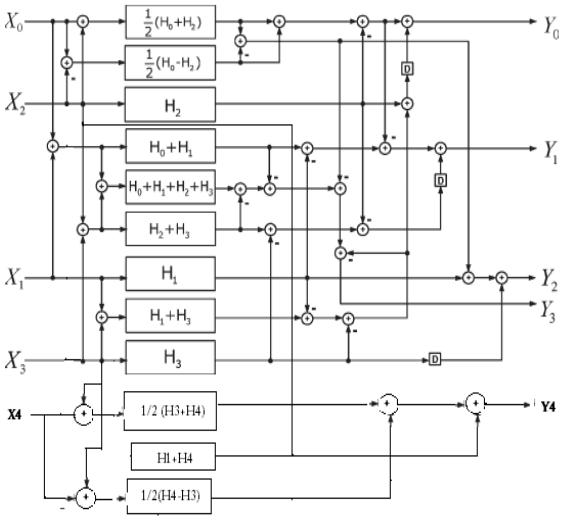
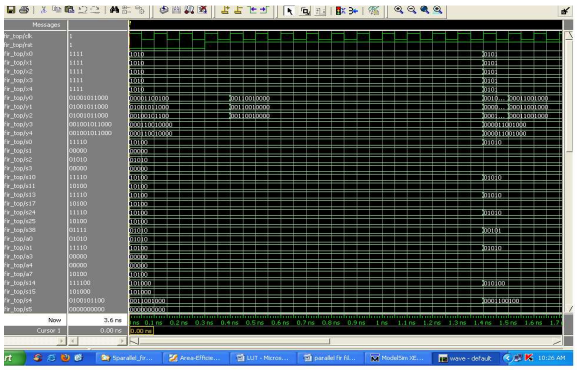


Fig 5 .Proposed five-parallel FIR filter implementation.

Result

	LUT	SLICES	DELAY (ns)
4 PARALLEL	304	171	28.798
5 PARALLEL	252	146	27.292

Simulation for Five Parallel FIR Filter



Conclusion

This paper proposes new parallel FIR filter structures, which are beneficial to symmetric coefficients in terms of the hardware cost, under the condition that the number of taps is a multiple of 2 or 3. The 5 parallel FIR structures gives low area and high speed compare to existing 4 parallel architecture , exploit the inherent nature of symmetric coefficients reducing half the number of multipliers in sub filter section at the expense of additional adders in preprocessing and post processing blocks. Exchanging multipliers with adders is advantageous because adders weigh less than multipliers in terms of silicon area. Due to reduction of multipliers, will get low area and high speed fir filter.

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